REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-3 and 5-6 are presently active in this case, Claim 1 having been amended by the present amendment, and Claims 7-10 having been previously withdrawn from consideration as directed to a non-elected invention.

In the outstanding Official Action, Claims 1-3, 5 and 6 are rejected under 35 U.S.C. §102(e) as anticipated by Appenzeller et al. (U.S. Pat. Pub. 2004/0120183 A1, herein "Appenzeller").

In light of the outstanding rejection on the merits, Claim 1 has been amended to clarify the claimed invention and thereby more clearly patentably define over the cited prior art. Support for the changes to Claim 1 is found, for example, at page 23, line 12 to page 24, line 20 of the specification. No new matter has been added.

Briefly recapitulating, Claim 1 is directed to a method of manufacturing a semiconductor device equipped with a capacitor in which a dielectric film is used, wherein a conductive complex oxide having an exposed top surface is used as a mask material when the dielectric film is subjected to reactive ion etching, and the mask material, which is in direct contact with the dielectric film, is used as an upper electrode of the capacitor after the reactive ion etching is performed.

In a non-limiting example described in the present specification,[1] a hard mask (for processing of the upper electrode) 11 is formed as shown in FIG. 2B, and upper SRO electrode (which serves as both an upper electrode and a hard mask) 12 (conductive complex oxide) is subjected to RIE as shown in FIG. 2C. The hard mask 11 disappears when RIE is performed. In other words, the top surface of the upper SRO electrode 12 is exposed. PZT

[1] Present specification at page 23, line 12 to page 24, line 20.

film 13 (dielectric film) is subjected to RIE, using the pattern of the upper SRO electrode 12 as a mask (refer to FIG. 2D). As a result, the width of the upper SRO electrode 12 (which is the mask) defines the width of the PZT film 13, and the edge portions of the surface of the exposed upper SRO electrode 12 are etched.

In contrast, the layer (PZT) 106 (dielectric film) of Appenzeller is etched together with upper electrode layer (SRO layer) 107 and isolation layer 108,[2] in a state where the isolation layer 108 is deposited on top of the upper electrode layer (SRO layer) 107.

In other words, in Appenzeller, the top surface of the upper electrode layer (SRO layer) 107 is not exposed. Further, the SRO layer does not define the shape of the dielectric film below it. The uppermost layer of the upper laminated structure functions as a mask.

Therefore, Appenzeller does not teach or suggest that a conductive complex oxide having an exposed top surface is used as a mask material when a dielectric film is subjected to reactive ion etching, and that the mask material, which is in direct contact with the dielectric film, is used as an upper electrode of the capacitor after the reactive ion etching is performed, as is recited in Claim 1.

Accordingly, from the above discussion, it is respectfully submitted that amended Claim 1 and Claims 2-3 and 5-6 dependent therefrom, patentably define over the cited Appenzeller reference.

[2] Appenzeller , paragraph [0036]

Consequently, in view of the present amendment and in light of the above comments, no further issues are believed to be outstanding, and the present application is believed to be in condition for allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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